Amendments to the Claims

The listing of claims will replace all prior versions and listings of claims in the application:

1-3. (canceled)

4. (previously presented) An apparatus for higher radix binary multiplication of a multiplicand by a multiplier to form a resultant product, said apparatus comprising:

means for recoding the multiplier into a plurality of primary digits in a primary radix;

means for recoding each of said primary digits into respective secondary digits in a second plurality of digits in a secondary radix;

means for generating a partial product of each secondary digit and said multiplicand, the partial products for the respective secondary digits collectively comprising a first plurality of partial products;

means for partitioning said first plurality of partial products into a plurality of parts and reducing each said part to respective values;

means for generating a second plurality of partial products, each partial product of said second plurality of partial products comprising the product of a respective value of a respective part and of a term dependent on said respective part and the secondary radix; and

means for reducing the second plurality of partial products to said resultant product.

5. (previously presented) The apparatus according to claim 4, wherein said primary radix is 32, and said secondary radix is 7, and said second number of digits in said secondary radix is 2, and said first plurality of partial products is partitioned into 2 parts.

6. (previously presented) The apparatus according to claim 4, wherein said primary radix is 256, and said secondary radix is 11, and said second number of digits in said secondary radix is 3, and said first plurality of partial products is partitioned into 3 parts.

7. (previously presented) The apparatus according to claim 4, wherein said means for partitioning reduces said respective values for each said part into a redundant binary format.

8. (previously presented) A method for higher radix binary multiplication, said method comprising the steps of:

receiving a multiplier and a multiplicand;

recoding the multiplier by extracting bits from the multiplier and obtaining first recoded digits from a first conversion table;

recoding the multiplier by extracting bits from the multiplier and obtaining second recoded digits from a second conversion table;

generating first partial products by selecting the first recoded digits in a Booth 4 partial product generator;

generating second partial products by selecting the second recoded digits in a Booth 8 partial product generator;

adding the first partial products to form a first result and multiplying the first result by 7 to form a second result;

adding the second partial products to form a third result; and

adding the second result and the third result to form a final result.

9. (previously presented) The method of claim 8, wherein the multiplier and the multiplicand are 64-bit values and the final result is a 128-bit value.

10. (previously presented) The method of claim 8, wherein the step of recoding to form the first recoded digits extracts 13 6-tuples of bits and the step of recoding to form the second recoded digits extracts 13 6-tuples of bits.

11. (previously presented) An apparatus for higher radix binary multiplication, said apparatus comprising:

means for receiving a multiplier and a multiplicand;

means for recoding the multiplier by extracting bits from the multiplier and obtaining first recoded digits from a first conversion table;

means for recoding the multiplier by extracting bits from the multiplier and obtaining second recoded digits from a second conversion table;

means for generating first partial products by inputting the first recoded digits and the multiplicand into a Booth 4 partial product generator;

means for generating second partial products by inputting the second recoded digits and the multiplicand into a Booth 8 partial product generator;

means for adding the first partial products to form a first result and multiplying the first result by 7 to form a second result;

means for adding the second partial products to form a third result; and

12. (previously presented) The apparatus of claim 11, wherein the multiplier and the multiplicand are 64-bit values and the final result is a 128-bit value.

13. (previously presented) The apparatus of claim 11, wherein the means for recoding to form the first recoded digits extracts 13 6-tuples of bits and the means for recoding to form the second recoded digits extracts 13 6-tuples of bits.

14. (previously presented) An apparatus for higher radix binary multiplication, said apparatus comprising:

a plurality of recoders;

a plurality of Booth 4 partial product generator selectors, connected to the recoders;

a plurality of Booth 8 partial product generator selectors, connected to the recoders;

an adder connected to the Booth 4 partial product generator;

an adder connected to the Booth 8 partial product generator selector;

a multiplier connected to the adder connected to the Booth 4 partial product generator; and

a carry propagate adder, connected to the adders and said multiplier.

15. (previously presented) A method for higher radix binary multiplication, said method comprising:

receiving a multiplier and a multiplicand;

recoding the multiplier by extracting bits from the multiplier and obtaining first recoded digits from a first conversion table;

recoding the multiplier by extracting bits from the multiplier and obtaining second recoded digits from a second conversion table;

multiplying the multiplicand by 7 to form a first result;

generating first partial products by selecting the first result in a Booth 4 partial product generator;

generating second partial products by selecting the second recoded digits in a Booth 8 partial product generator; and

adding the first partial products and the second partial products to form a final result.

16. (previously presented) The method of claim 15, wherein the multiplier and the multiplicand are 64-bit values and the final result is a 128-bit value.

17. (previously presented) The method of claim 15, wherein the step of recoding to form the first recoded digits extracts 13 6-tuples of bits and the step of recoding to form the second recoded digits extracts 13 6-tuples of bits.

18. (previously presented) An apparatus for higher radix binary multiplication, said apparatus comprising:

means for receiving a multiplier and a multiplicand;

means for recoding the multiplier by extracting bits from the multiplier and obtaining first recoded digits from a first conversion table;

means for recoding the multiplier by extracting bits from the multiplier and obtaining second recoded digits from a second conversion table;

means for multiplying the multiplicand by 7 to form a first result;

means for generating first partial products by inputting the first result and a first recoded digit into a Booth 4 partial product generator;

means for generating second partial products by inputting the first result and respective second recoded digits into respective Booth 8 partial product generators; and

means for combining the first partial products and the second partial products to form a final result.

19. (previously presented) The apparatus of claim 18, wherein the multiplier and the multiplicand are 64-bit values and the final result is a 128-bit value.

20. (previously presented) The apparatus of claim 18, wherein the means for recoding to form the first recoded digits extracts 13 6-tuples of bits and the means for recoding to form the second recoded digits extracts 13 6-tuples of bits.

21. (previously presented) An apparatus for higher radix binary multiplication, said apparatus comprising:

a plurality of recoders;

a plurality of Booth 4 partial product generator selectors, connected to the recoders;

a plurality of Booth 8 partial product generator selectors, connected to the recoders;

a multiplier connected to the Booth 8 partial product generator selectors; and

a carry propagate adder, connected to the Booth 4 partial product generator selectors and the Booth 8 partial product generator selectors.